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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Hongjiang Song	§	Art Unit:	2631
Serial No.:	09/473,740	§	Examiner:	Don Nguyen Vo
Filed:	December 28, 1999	§		
Title:	Synchronization Detection Architecture for Serial Data Communication	§	Docket No.	ITL.0327US (P8030)

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REPLY BRIEF

Dear Sir:

Applicant submits the following reply to the Examiner's Answer.

I. GROUPING OF THE CLAIMS

Claims 1-7 are grouped together; claims 8-14 are grouped together; and claims 15-20 are grouped together.

Date of Deposit: August 11, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop ~~Appeal~~ **Brief-Patents**, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Janice Munoz

II. REPLY TO EXAMINER'S ARGUMENTS

The Examiner has not shown where the prior art contains the alleged suggestion or motivation to combine alleged Applicant's admitted prior art (herein called the "AAPA") in view of Lang to derive the claimed invention. Instead, the Examiner improperly combines the alleged AAPA and Lang in a piecewise fashion based on the hindsight gleaned from the claimed invention to derive the § 103 rejections.

Even if a suggestion or motivation is present in the prior art for the hypothetical combination of the alleged AAPA and Lang, this hypothetical combination does not produce the claimed invention. In other words, neither Lang nor the AAPA teaches or suggests the solution that is presented by the claimed invention.

As pointed out in the Appeal Brief, Lang merely teaches that a shift register is used to detect a synchronization field. This shift register does not buffer to accommodate a rate difference between incoming and outgoing data. Therefore, assuming, for purposes of argument, that the alleged AAPA and Lang are combined, this hypothetical combination arguably produces the repeater 5 of Fig. 1 (of the alleged AAPA) in which Lang's shift register is used for the synchronization detection circuit 18. However, the Examiner has failed to show where the prior art contains the alleged suggestion or motivation to move Lang's shift register into the data recovery circuit 16 (instead of the synchronization detection circuit 18, for example) and use this shift register to buffer different rates of data. Instead, the Examiner improperly modifies the alleged AAPA in view of Lang based on the hindsight that is gleaned from the claimed invention.

"Obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966). Instead, a *prima facie* case of obviousness

requires the Examiner to show where the prior art contains a suggestion or motivation to modify or combine references to derive the claimed invention.

Additionally, the Examiner fails to address Applicant's contention that the alleged AAPA teaches away from the claimed invention and therefore, cannot be used in an obviousness rejection. A reference that teaches away from the claimed invention cannot be combined with another reference in an obviousness rejection of the claimed invention. M.P.E.P. § 2145.X.B.

For at least the reasons that are set forth above and in the Appeal Brief, the Examiner has not established a *prima facie* case of obviousness for any of the claims. Therefore, Applicant maintains that the § 103 rejections of claims 1-20 are in error and should be reversed.

Respectfully submitted,

Date: August 11, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field.

2. The method of claim 1, further comprising:

after the buffering, communicating the bits to a second serial bus to form the outgoing data.

3. The method of claim 2, wherein the communicating comprises:

selectively enabling a transmitter based on the detection.

4. The method of claim 3, further comprising:

determining whether the indication of the bits indicates valid bit logic levels; and

further basing enablement of the transmitter on the determination.

5. The method of claim 1, wherein the receiving comprises:

receiving an indication of at least one analog signal from the first serial bus; and

converting the indication of said at least one analog signal into indications of at least some of the bits.

6. The method of claim 1, wherein the buffering comprises:

passing the bits through a delay line.

7. The method of claim 1, wherein the detecting comprises:

comparing at least some of the bits to an indication of a predetermined bit pattern.

8. A repeater comprising:

a data recovery circuit to receive an indication of bits of incoming data from a first serial bus and buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data; and

a synchronization detection circuit coupled to the data recovery circuit to detect, while the data recovery circuit buffering the bits, whether at least some of the bits indicate a synchronization field.

9. The repeater of claim 8, further comprising:

a transmitter to receive an indication of the bits from the data recovery circuit and use the indication from the data recovery circuit to communicate the bits to a second serial bus to form the outgoing data.

10. The repeater of claim 9, wherein the synchronization circuit selectively enables the transmitter based on the detection by the synchronization detection circuit.

11. The repeater of claim 10, further comprising:

a squelch detection circuit to indicate whether valid bit logic levels are present on the first serial bus,

wherein the synchronization circuit selectively enables the transmitter further based on the indication from the squelch detection circuit transmitter.

12. The repeater of claim 10, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.

13. The repeater of claim 10, wherein the data recovery circuit comprises:

a delay line to delay the bits by multiple cycles of a clock signal.

14. The repeater of claim 10, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

15. A system comprising:

a first serial bus;

a second serial bus; and

a repeater coupled to the first and second serial busses to receive an indication of bits of incoming data from the first serial bus, and concurrently buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data and detect whether at least some of the bits indicate a synchronization field.

16. The system of claim 15, wherein the repeater comprises:

a receiver to receive an indication of bits of the incoming data from the first serial bus; and

a transmitter to communicate the bits to a second serial bus to form the outgoing data.

17. The system of claim 16, further comprising:

a synchronization circuit to detect the synchronization field and selectively enable the transmitter in response to the detection.

18. The synchronization circuit of claim 16, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

19. The system of claim 15, further comprising:

a squelch detection circuit to enable communication to the second serial bus based on whether valid bit logic levels are present on the first serial bus.

20. The system of claim 15, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.